MRAM Developer Day
2018 MRAM Update

Barry Hoiberman
Disclaimer

- Observations and opinions…

- >35 years experience in wide variety of memory
- >12 years experience in MRAM
- 2012-2017 CEO/Chairman at Spin Transfer Technologies, Inc.
  - 2006-2012 Crocus Technology
## MRAM at the Gate

<table>
<thead>
<tr>
<th>Year</th>
<th>4Mbit</th>
<th>16Mbit</th>
<th>64Mbit</th>
<th>256Mbit</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;2007</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Devices

<table>
<thead>
<tr>
<th>Year</th>
<th>GMR</th>
<th>MTJ</th>
<th>MTJ</th>
<th>MTJ</th>
<th>MTJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;2007</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td></td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
</tr>
<tr>
<td>2010</td>
<td></td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
</tr>
<tr>
<td>2017-18</td>
<td></td>
<td></td>
<td>MTJ</td>
<td>MTJ</td>
<td>MTJ</td>
</tr>
</tbody>
</table>

### Scaling

<table>
<thead>
<tr>
<th>Year</th>
<th>&lt;2007</th>
<th>2008</th>
<th>2010</th>
<th>2012</th>
<th>2017-18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Units</td>
<td></td>
<td>2008</td>
<td>2010</td>
<td>2012</td>
<td>2017-18</td>
</tr>
<tr>
<td>~180nm</td>
<td></td>
<td>180nm</td>
<td>130nm</td>
<td>90nm</td>
<td>28-40nm</td>
</tr>
</tbody>
</table>

### MTJ Types
- GMR
- MTJ Toggle
- MTJ Spin Torque

### Notes
- Scaling Barrier
- ~ 10^8 units shipped
3rd generation STT MRAM cannot simultaneously provide speed, endurance, and retention for high speed SRAM application.
Four Generations of Production MRAM

- Not Scalable beyond 130nm (write power)

Gen.2: Planar STT (2012)
- Not Scalable beyond 65/40 nm (retention)

Gen.3: Perp. STT (2018)
- Fully scalable Endurance-Retention-Speed tradeoff
  → Limited persistence and/or endurance and/or speed

Future Gen.4: SOT
- Fully scalable
- Infinite endurance
- High intrinsic speed
- Persistent RAM compatible

SOT solves STT shortfalls for RAM applications
Manufacturing Ramp at Foundries

- Samsung, TSMC, Global Foundries in ramp up in 22-28nm insertions
  - In logic processes as ‘embedded memory’ in SOC
- STT-MRAM introduction primarily as ‘roadmap substitution’ for embedded NOR Flash replacement
  - Plus some use as ‘pseudo’ RAM
    - Compromises on speed, endurance, retention
    - Production starts 2018-2019
- STT-MRAM not applicable as general purpose embedded SRAM replacement
Essential 300mm tools with suitable wafer throughput and technical capability reaching availability

- Applied Materials, TEL, Canon/Anelva
- Magnetic film deposition and etch are principle requirements

Yield and other process control converging on manufacturable, but not yet equal to incumbent memory types
Emerging Memory Technology

Market/Production Momentum

MRAM

PHASE CHANGE

ReRAM

NANOTUBE
Discrete MRAM in Storage
‘The Low Hanging Fruit’

RAID systems
- 5-10+ memories per RAID system controller
- $100-1000 per system
- 5M+ units/year

SSD / HDD controller
- R/W cache, Logical/Physical Address Table, etc...
- $1-4 per drive
- $50-100 per system in high end storage system
- 500M+ units per year

“Front End” multi-Gb buffer
- in mission critical high performance SDD
- 1-2 memories per drive
- $10-20 per drive
- 150M units per year

Critical mission: ‘Protect Data in Flight’
Requires: Speed and Endurance of DRAM, with instantaneous power-off data retention
‘High Impact’ MRAM Application Promise

Top 10 List

1. >1 Million IOP SSD
2. Unified Memory (XIP) Microcontroller
3. Persistent Cache for Mobile CPU
4. Big-Capacitor-Free Performance SSD
5. SOC Embedded SRAM Replacement
6. SOC Embedded Flash Replacement
7. ‘High Training Rate/Low Training Energy’ NVM Memory for AI
8. Persistent Cache for Storage System
9. Rad Hard High Density Flash Replacement
10. ‘High Endurance’ Flash Gap
‘High Impact’ MRAM Application Promise

Top 10 List – Near Term Impact Predictions

1. >1 Million IOP SSD
2. Unified Memory (XIP) Microcontroller
3. Persistent Cache for Mobile CPU
4. Big-Capacitor-Free Performance SSD
5. SOC Embedded SRAM Replacement
6. SOC Embedded Flash Replacement
7. ‘High Training Rate/Low Training Energy’ NVM Memory for AI
8. Persistent Cache for Storage System
9. Rad Hard High Density Flash Replacement
10. ‘High Endurance’ Flash Gap
Editorial

Why new chip memory is so hard…

- Practical equipment/manufacturing barrier
  - Production fabs don’t do development and cost $5-10 billion
  - Full development today requires >$200 million
    - New physical structures ‘manufacturability’ isn’t known till late in development cycle
- Multi-dimensional ‘chicken & egg’ situation

- Takeaway: It’s HUGE that leading CMOS foundries have installed production equipment, invested in processes, and are on the threshold of MRAM production
Why new chip memory is so hard…

- Matching new technology manufacturing yield/performance curve to design expectations
  - Combining well-known CMOS yield characteristics with ambiguous and optimistic ‘new device’ yield statistics is hard
    - Cross-functional engineering teams universally underestimate

Takeaway: Teams that focus on bridging both the ‘yield curve gap’ with margin and the ‘cross-functional interdependency gap’ will win in this emerging market
Free-format slide title
Some Notes about this template

- The first action you should take is to save this presentation
  - You have opened a design template (.pot)
    - Need to save as .ppt
- A master exists for:
  - Slides
  - Handouts - default is 3 to a page
    - You can print a different number, but no guarantees about appearance
Some Notes about this template

- The first action you should take is to save this presentation
  - You have opened a design template (.pot)
    - Need to save as .ppt
- A master exists for:
  - Slides
  - Handouts - default is 3 to a page
    - You can print a different number, but no guarantees about appearance

Notes
Free-format slide title