



# MRAM Brings Native Persistence to Memory Workloads

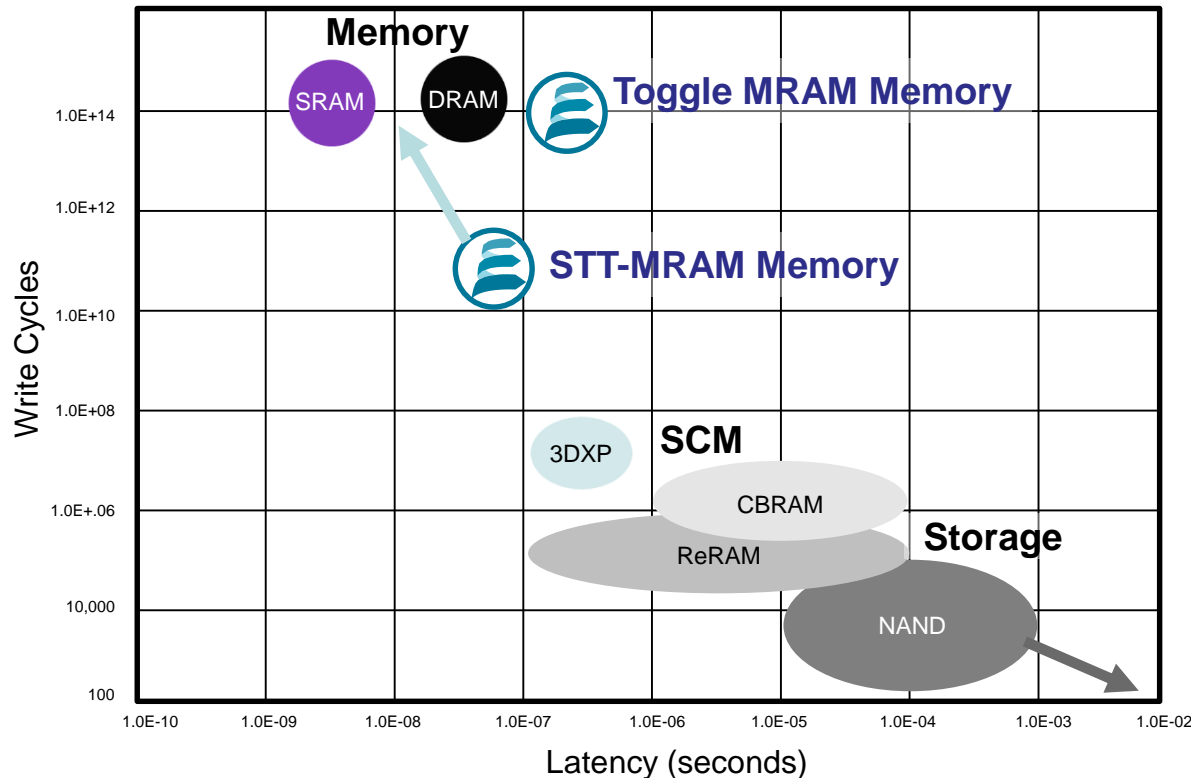
James Singer

Director of Application Engineering  
Everspin Technologies

MRAM Development Track #1  
Room: GAMR1, 3:30 - 4:45PM  
August 6<sup>th</sup>, 2018



# For Reference: Legacy Discrete Memory Solutions



**MRAM combines performance of memory with persistence of storage**

- High Performance: DRAM-class write performance
- Non-Volatile: Maintains memory without power
- Fast Read/Write Speeds: Similar to SRAM & DRAM
- Superior Durability: Survives memory workloads
- No Refresh: Data requires no charge



# ST-DDR3 design considerations

- Timing
- Smaller page sizes
- Power Up
- Power Down
- Performance
- ECC Algorithm
- Endurance



# Timing changes (row timings only)

Parameter	Symbol	DDR3-1333 DRAM		ST-DDR3-1333 STT-MRAM	
		ns (min)	ck (min)	ns (min)	ck (min)
CAS Latency	tCL		10		10
CAS Write Latency	tCWL		7		7
ACTIVE to internal READ or WRITE delay time	tRCD	15	10	95	64
Precharge command period	tRP	15	10	66	44
ACTIVE to ACTIVE command period	tRC	51	34	170	114
ACTIVE to Precharge command period	tRAS	36	24	103	69
Write Recovery, WRITE to Precharge delay time	tWR	15	10	15	10
ACT to ACT Command Period, different banks	tRRD	6	4	30	20
Four ACTIVE Window	tFAW	30	20	120	80
REFRESH to ACT command delay (1Gb to 8Gb)	tRFC		74 – 234		Not Used

## tCL-tRCD-tRP-tRAS

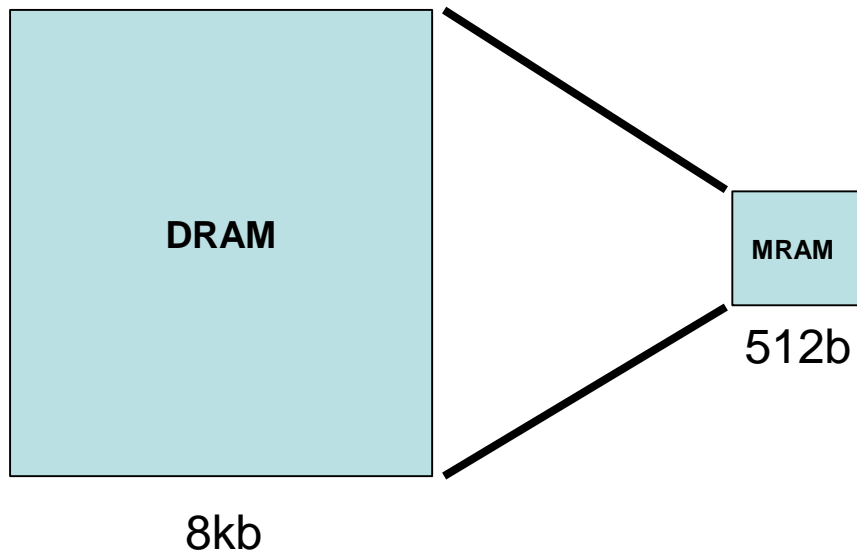
(DDR3) 10-10-10-24

(ST-DDR3) 10-64-44-69

- Extended row address timings
- Refresh is not required
- CAS timings remain the same



## Page sizes are 16x smaller for ST-DDR3



- DRAM Page sizes are optimized around REFRESH
- MRAM does not use REFRESH
- MRAM Page sizes are optimized to minimize power

### Fewer Column Address bits

- DRAM Column Addr = 10b
- MRAM Column Addr = 6b



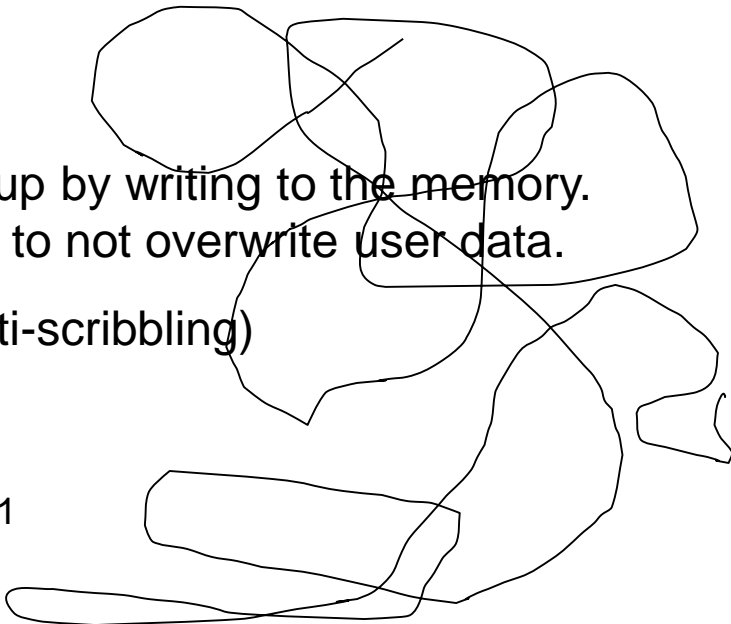
## Power-up

DRAM Controllers will calibrate after power-up by writing to the memory.  
With persistent memory, care must be taken to not overwrite user data.

What is NOMEM Mode? (also known as Anti-scribbling)

- 
- 
- 
- 1. Mode Register 2 (MR2) – 0x0110 MR2[8] = 1
- 2. Mode Register 3 (MR3) – 0x0000
- 3. Mode Register 1 (MR1) – 0x0044
- 4. Mode Register 0 (MR0) – 0x0b60
- 5. After Calibration and before normal operation
- 6. Mode Register 2 (MR2) – 0x0010 MR2[8] = 0

•  
•  
•





# Power-down ...with *Guaranteed Persistence*

Scram /skram/ - leave or go away from a place quickly.

## Why:

- To ensure all important and write committed data is persistent

## When:

- Power rail begins to slump (+12V)
- Over voltage
- Over current
- Over temperature

## What:

- open pages
- buffers
- write committed data in DRAM
- anything you deem important



## SCRAM Routine

1. Stop accepting any new commands
2. Process all pending commands
3. Complete all pending MRAM writes
  - a) **NOTE: To guarantee persistence, executing a Precharge (PRE) or Precharge All (PREA) command must be performed to move data in to the persistent memory array.**
4. Communicate that ALL pending writes are complete (assert `SCRAM_complete`)
5. It is now safe to power off MRAM without losing data (**Guaranteed persistence**).



# ECC



*Application Note*

## ECC Considerations for STT-MRAM Designs

---



To achieve a robust and reliable persistent memory design with STT-MRAM, designers need to also consider the internal architecture of STT-MRAM devices. In this application note we will

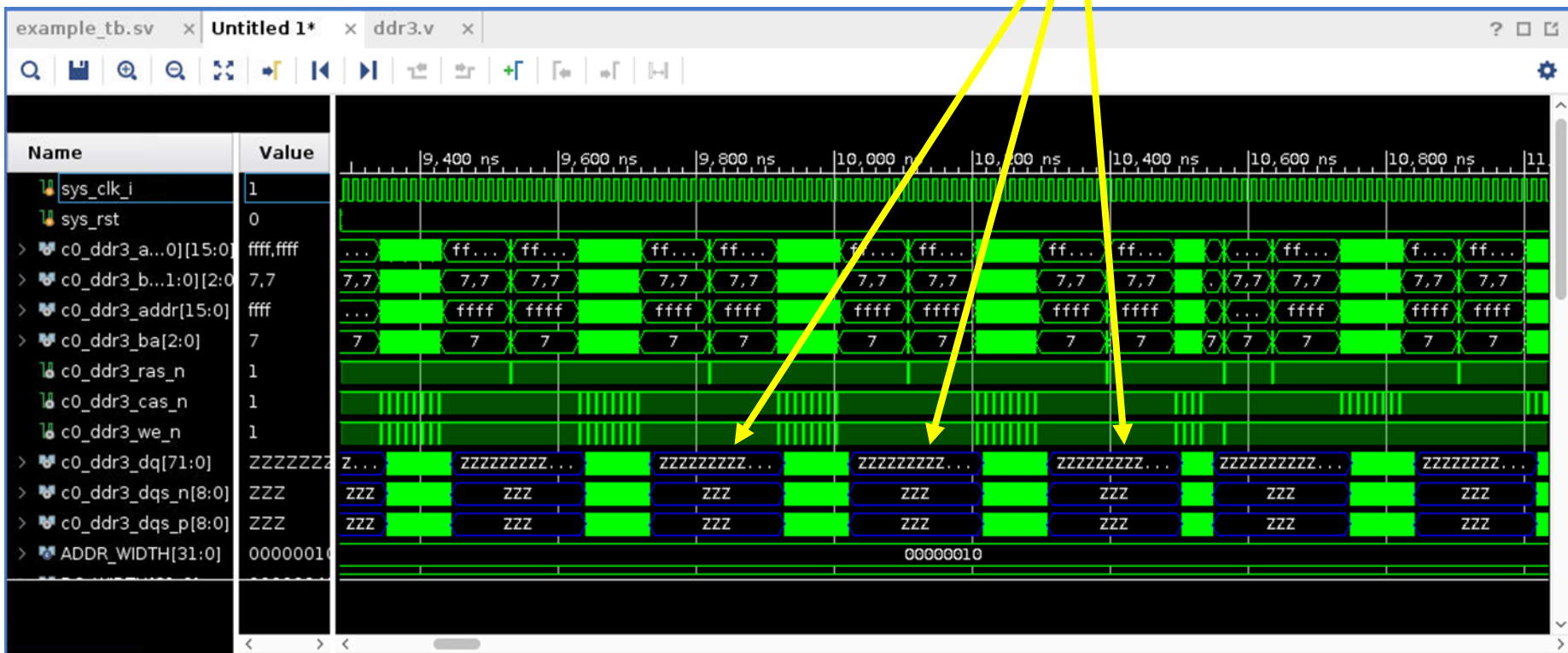
Any robust and reliable design will require either SEC or DEC





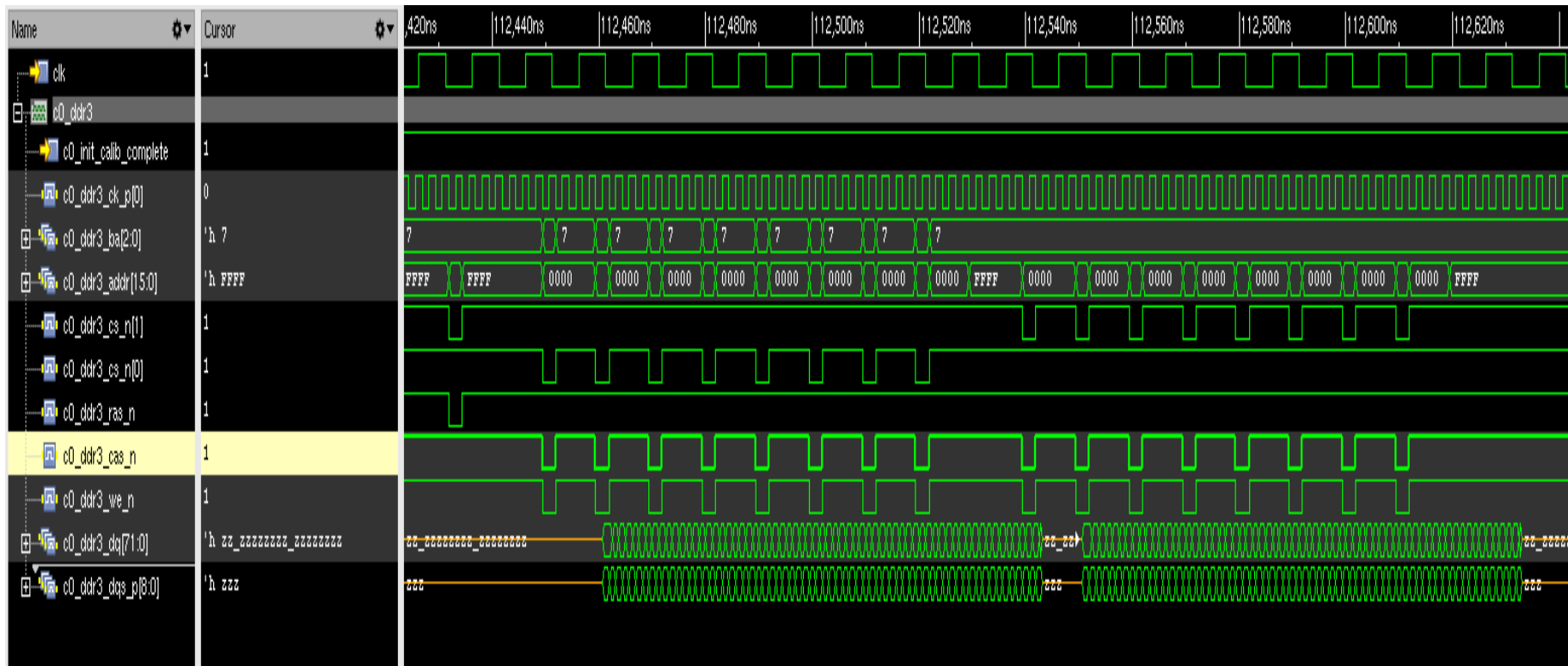
# Performance

Note the Large gaps between bursts





# Performance – improved bus utilization

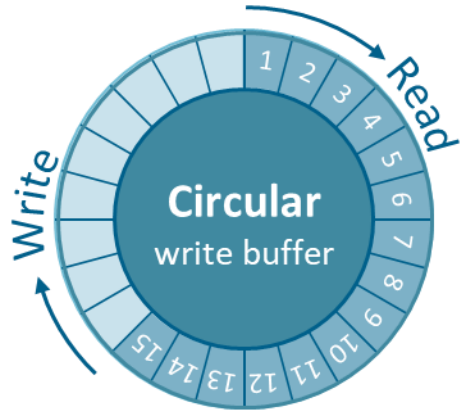
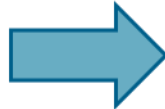




# Endurance

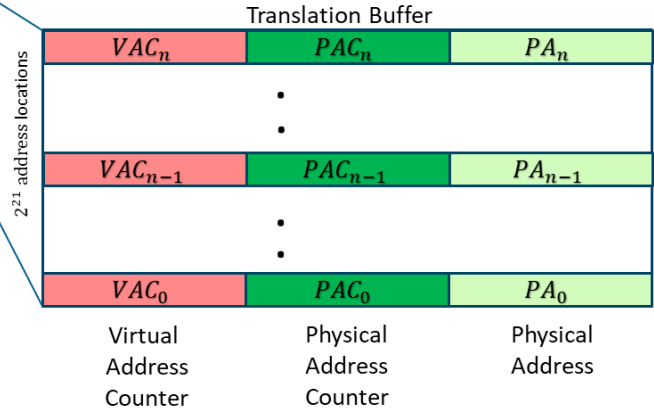
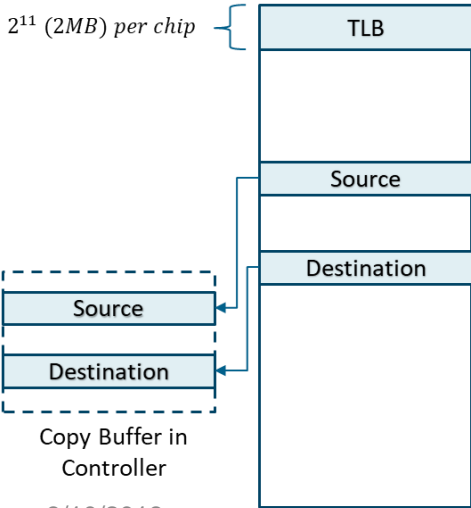
### Incoming Data

- Variable Rate
- Bursts
- Latency sensitive



### Modified TLB (enhanced endurance)

$2^{21}$  (2MB) per chip



Circular write buffer

Or

Custom Endurance enhancement algorithm

# Everspin is eager to help

- ✓ Timing
- ✓ Smaller page sizes
- ✓ Power Up
- ✓ Power Down
- ✓ Performance
- ✓ ECC Algorithm
- ✓ Endurance





What does it mean to be persistent?

Thank you