Magnetic Migration into the Memory Hierarchy

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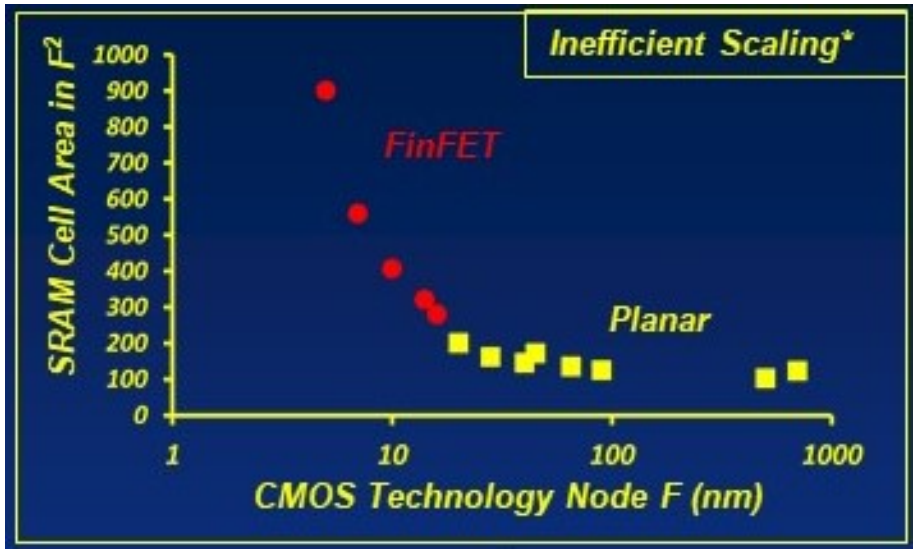
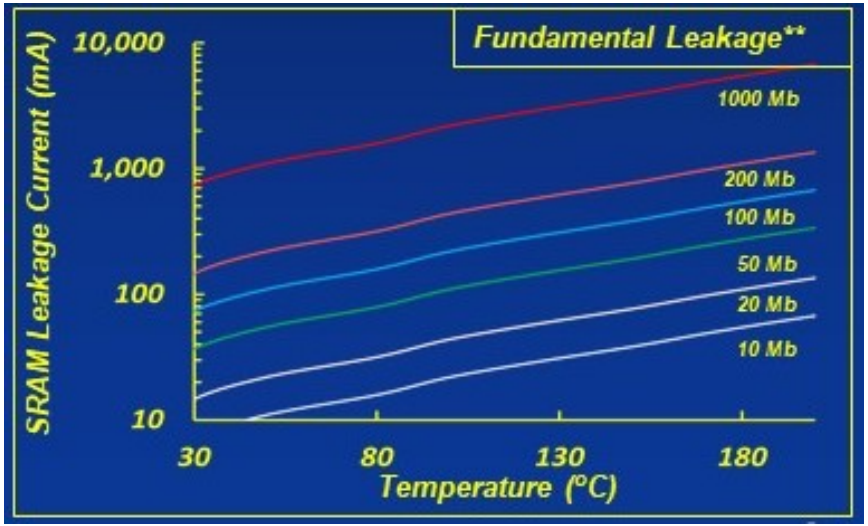
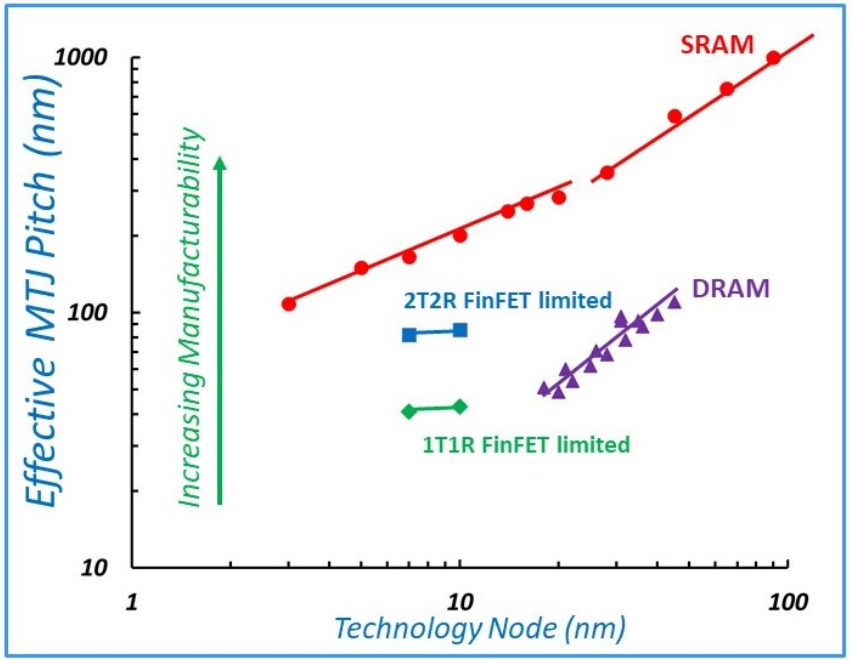
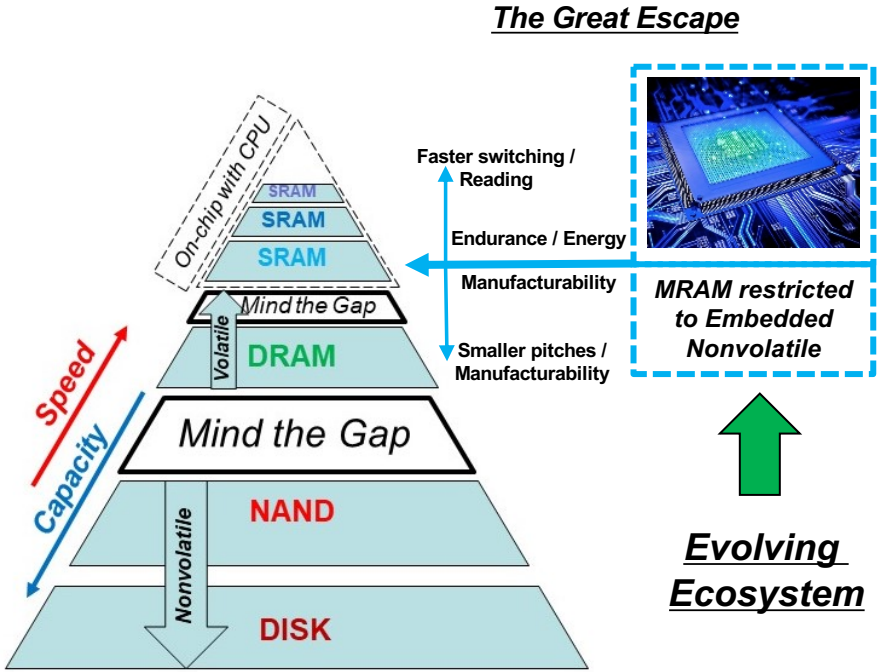
The Looming SRAM Catastrophe



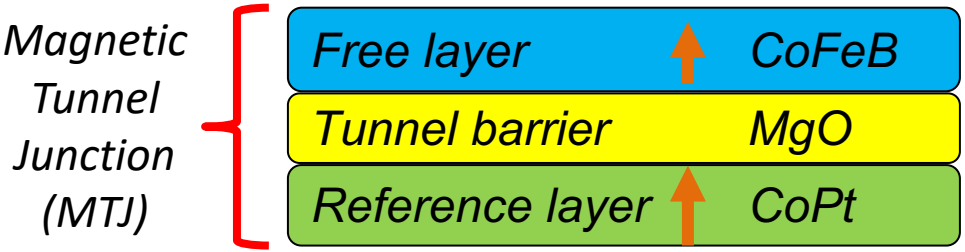


Effective Pitch as a Roadmap Guide to Magnetic Migration

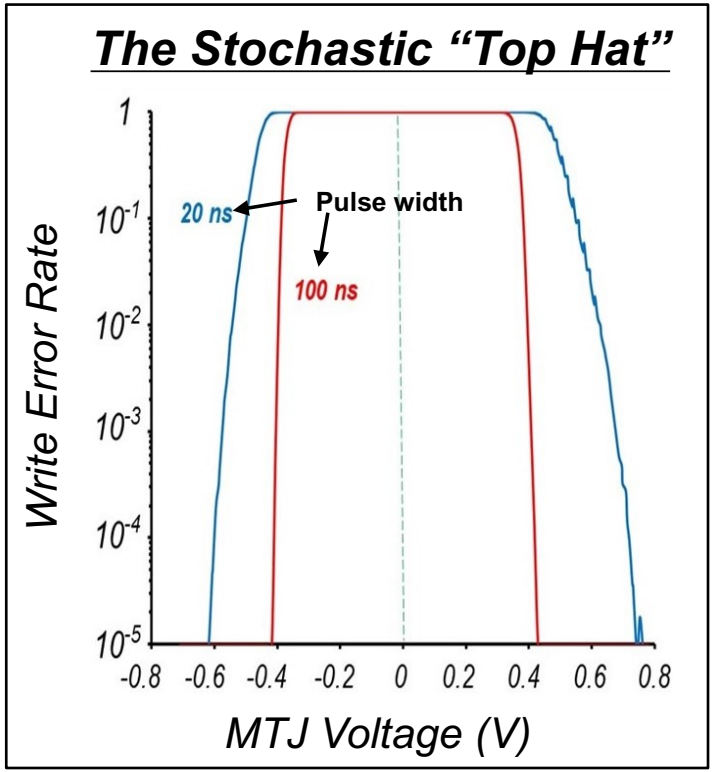




STT-MRAM: A Unique Endurance Conundrum

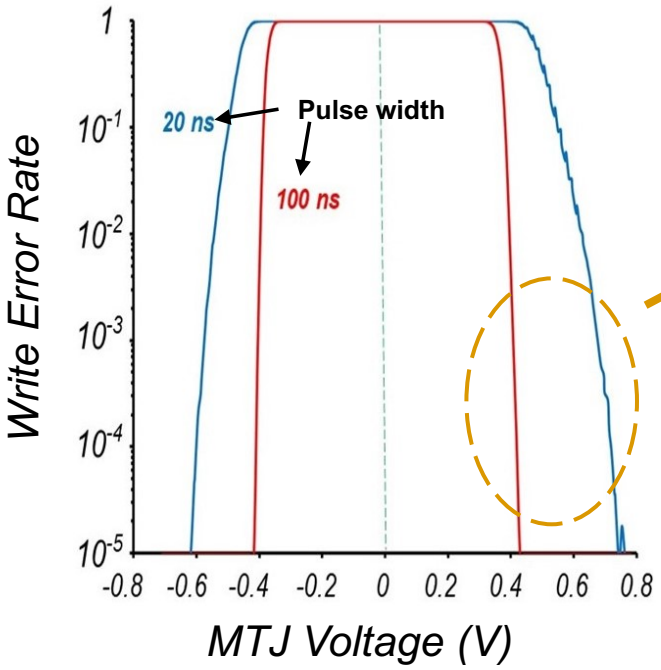


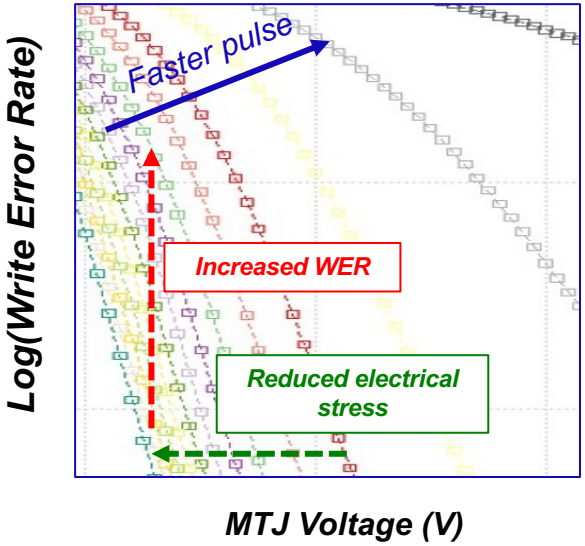
- ***Low Write Error Rate needs large tunnel current***
  - *Limits endurance due to oxide wear out mechanism*
- ***High endurance with low Write Error Rate needs reduced tunnel current***
  - *Make Free Layer magnetically less "stiff"*
  - *Reduce MTJ area*
  - *Use special design techniques -* ***The "Engine"***



The Physics of the Engine

The Stochastic "Top Hat"





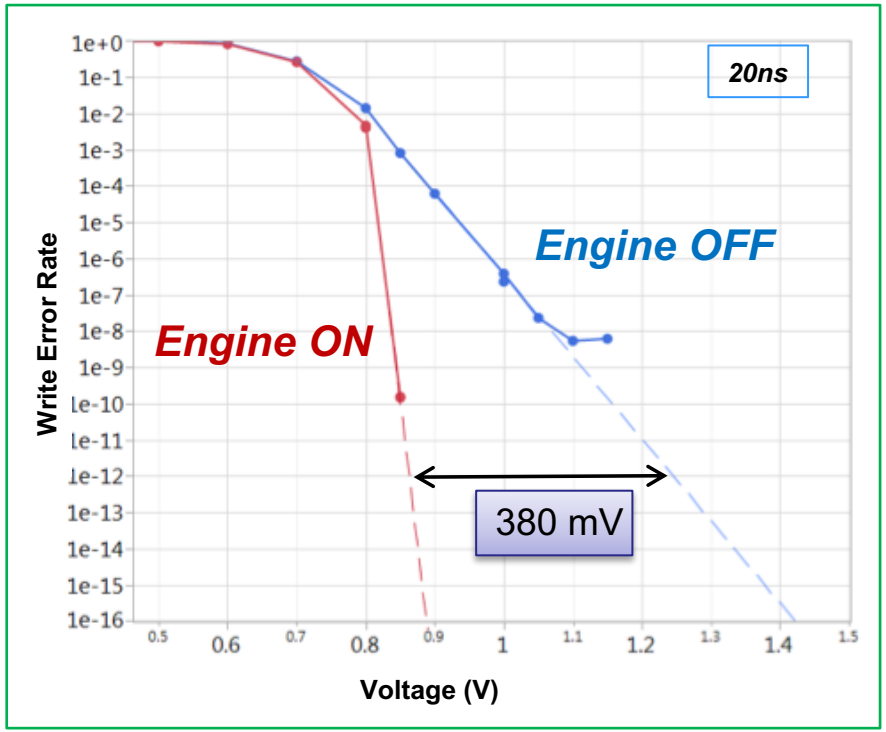
Proprietary Circuit Design *allows* ***reduced electrical stress***

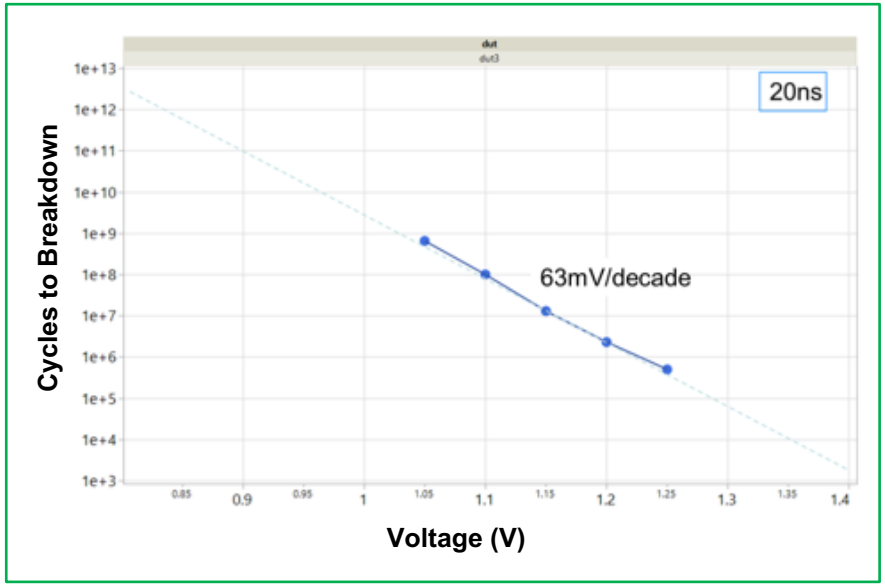
- *Results in large endurance increase* ***(~ 6 orders of magnitude)***

Circuit Deals *with resultant* ***Write Error Rate increase***

- *Managed transparently to the user*
- *No change in latency*
- *Allows for faster pulses at high endurance*

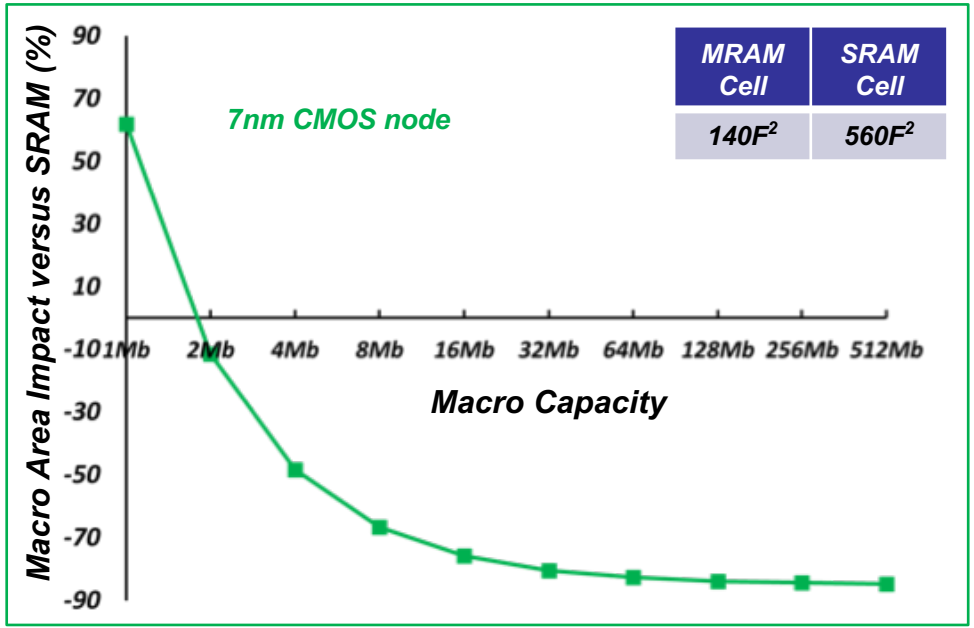
Data from Emulated Engine





~ 6 orders of magnitude endurance boost

The Performance, Energy and Cost Advantage



- Dramatic area impact
- Maximize large on-chip cache and memory capacity
- Allows persistence on-chip
- Reduces DRAM accesses
- ~ Zero array leakage
- Symmetric Read/Write

Conclusions

- STT-MRAM as embedded NV is an evolving ecosystem
- A “Great Escape” to an SRAM/DRAM replacement needs low Write Error Rates and high endurance (> 10^{13})
- The “ENGINE” provides the path
- Effective pitch defines the product strategy
  - The looming SRAM catastrophe is the first target
  - DRAM and Gap-Filling Storage Class Memory are next